1) Micro-operations for ADIW ZH:ZL, 32. 5 cycles for fetch and 6 cycles for execute. MDR is 8 bits and AC, SP, PC, IR, and MAR are 16 bits.

Fetch cycle

Step 1: MAR ← PC;

Step 2: MDR ← M(MAR), PC ← PC+1 ; Get the high byte of the instruction and increment PC

Step 3: IR ← MDR ;

Step 4: MAR ← PC;

Step 5: MDR ← M(MAR), PC ← PC+1 ;

Execute cycle

Step 6: AC ← R30

Step 7: AC ← AC + MDR ; Add 32 to ZL

Step 8: R30 ← AC ; Write back to register file

Step 9: AC ← R31

Step 10: If (C==1) then AC ← AC +1 ; Increment ZH if there was a carry

Step 11: R31 ← AC ; Write it back to register file

2) Micro-operations for Icall. 6 Cycles for fetch and 8 cycles for execute. MDR is 8 bits and AC, SP, PC, IR, and MAR are 16 bits.

Fetch

1. MAR←PC
2. MDR←M(MAR),PC←PC+1
3. IR(15…8) ←MDR
4. MAR←PC
5. MDR←M(MAR),PC←PC+1
6. IR(7…)←MDR

Execute

1. MDR←PC(7…0)
2. MAR←SP
3. M(MAR) ←MDR,SP←SP-1
4. MDR←PC(15..8)
5. MAR←SP
6. M(MAR) ←MDR,SP←SP-1
7. PC(7…0)← R30
8. PC(15..8) ←R31

3)

4)